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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SINGH, DALIP K	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 02/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/341,633	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Remarks

1. This Office Action is in response to applicant's remarks dated March 3, 2005 in response to PTO Office Action dated December 3, 2004.

Applicant's arguments filed March 3, 2005 have been fully considered and they are persuasive. However, upon further consideration, a new ground(s) of rejection is made in view of US 5,043,714 to Perlman, 5,901,274 to Oh; US 5,706,478 to Dye; US 6,124,842 to Mizutome et al.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,859,649 to Yiu et al. in view of US 5,043,714 to Perlman.

a. Regarding claim 1, Yiu et al. **discloses** a main memory (system memory 30, Fig. 2); a data processing circuit (LCD control logic 61 consisting of cursor logic 62, frame rate control 64, and LCD interface 66, Fig. 2) which converts the data format of said display data into the data format of the screen display; a number of line memories (line buffer 60, Fig. 2;...Line buffer 60 essentially comprises two or more line buffers...col. 4, lines 11-12); a display control section (LCD control module 28;...uses both bus arbitration and data bursting to supply display data to line buffer 60 from system memory 30, as needed to refresh LCD screen 49...col. 4, lines 7-10; Fig. 2 and Fig. 3) which controls the transfer and storage of the display data from said main memory

(system memory 30) to said line memory (line buffer 60) and the readout of the necessary display data from said line memory (line buffer 60) to display it on the screen; and a main control section (CPU 22, Fig. 2) which controls the storage of said display data in said main memory (system memory 30, Fig. 2)(...the system memory is shared between the display controller and a central processing unit (CPU)...col. 1, lines 42-44; ...SIM 40 (System integration module) is connected to internal bus circuit 34 and can receive and transmit signals to data processing system 20 by way of internal bus circuit 34...col. 2, lines 19-26;...CPU 22 is connected to internal bus circuit 34 and may receive and transmit signals to each of the other module connected to internal bus circuit 34. CPU 22 may optionally receive and transmit signals external to data processing system 20 by way of SIM 40. The CPU is usually responsible for receiving, interpreting, and executing the software instructions used to control the data processing system...col. 2, lines 39-45), and the transfer of the stored information. However, Yiu et al. **is silent about** data format and storage address information transfer to said display control section, wherein said display control section reading out said display data by specifying the address of the display data for one line which has a possibility to be displayed on the screen to said main memory from which the display data is transferred, based on said stored information, causing said data processing circuit to perform the data transfer and select said line memory to store said display data. Perlman **discloses** memory that is used for storing the data representative of a plurality of objects to be displayed i.e., objects may be stored in a different number of locations and storage of attributes for each of the objects i.e., information such as screen position, object's location in the memory (col. 1, lines 64-67; col. 2, lines 1-13); and a line buffer controller controlling the loading of the data into the line buffer and the data can be different types of pixel data (col. 2, lines 14-34). Perlman **discloses** the RAM 35 (similar main memory of the

instant claim), having a configuration data section 36, and object dispatch table 37; and the object description data; and this would indicate where each object is stored within the memory RAM 35 (...one attribute for each object is a starting address pointer which points to the first line of display-data within the RAM 35...col. 5, lines 60-67; col. 6, lines 12-14;...one of the functional units of Fig. 5 or RAM 35 is responsive to the address on bus 58. The addressed data is thereby located and it is prepared for transmission on bus 60...simultaneous to the address generation on bus 58, the dispatcher couples a sequence of instructions (see fig. 22 and 23) which prepares the line buffer for the data about to be sent by the device responsive to the dispatcher's address...col. 8, lines 59-67; col. 9, lines 1-3). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Yiu with the feature "display control section reading out display data by specifying the address of the display data for one line to said main memory from which the display data is transferred, and selection of said line memory to store said display data" as taught by Perlman **because** this provides for data storage in an efficient contiguously accessible memory locations (col. 5, lines 7-21).

b. Regarding claim 2, Yiu et al. **discloses** wherein said display control section (LCD control module 28) controls the storage of the display data to be utilized repeatedly in said line memory (line buffer 60), said repeated display data is read out from said line memory (line buffer 60) by specifying the address thereof and displayed on the screen (...words are burst from system memory 30 to line buffer 60. At clock cycle t2, a base address, labeled "A0" is provided by screen DMA...Data signals labeled "D0", corresponding to base address A0, are read from system memory 30 and written to line buffer 60...the data burst continues from clock cycle t4 to clock cycle t9 for address signals A2-A7...col. 4, lines 35-50).

c. Regarding claim 3, Yiu et al. **discloses** cursor logic 62 that receives the display data and controls a location of a cursor on the display screen (...LCD control logic 61 pumps the display data through cursor logic 62, frame rate control 64, and LCD interface 66 to refresh the LCD display screen. Cursor logic 62 receives the display data and controls a location of a cursor on the display screen...col. 4, lines 65-67; col. 5, lines 1-10).

d. Regarding claim 9, Yiu et al. **does not disclose** line information showing in which line the data is to be used when storing the display data in said line memory, and the controlling the display of the data in such a manner that when reading data from said line memory, the line information is read out simultaneously and the data is displayed only when the line which uses said display data is the same with the line information. Perlman **discloses** for each frame of the display, dispatch table is transferred to the dispatcher 48. The dispatcher determines which objects have data for line 0 and then accesses this data from the RAM 35. The data is read from the RAM 35 and coupled to the bus 60 to the line buffer 50. The line buffer 50 composes line 0 from the data it receives for the various objects which extend to line 0 (col. 7, lines 38-60). Perlman further discloses dispatcher taking control of address bus 58 and couples an address on that bus which is the first address of the data for that line (which coincides with the current raster line of the display) of the object. The addresses data is thereby located and it is prepared for transmission on bus 60 (col. 8, lines 55-66). The dispatcher couples a sequence of instructions which prepares the line buffer for the data about to be sent by the device responsive to the dispatcher's address (col. 8, lines 66-68; col. 9, lines 1-4). In general, in operation one line of data for each object is read into the line buffer to compose a line of pixel data for the display (col. 2, lines 25-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to

modify the device as taught by Yiu et al. with the feature "line information being mated to the line which uses said display data resulting in efficient operation" as taught by Perlman (col. 12, lines 1-13).

4. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,859,649 to Yiu et al. in view of US 5,043,714 to Perlman as applied to claim 1 above, and further in view of US 5,901,274 B1 to Oh.

a. Regarding claim 4, Yiu et al. **disclose** a line buffer 60 that comprises two or more line buffers receiving display data readout from main memory (system memory 30) and **fails to disclose** a second buffer for storing the display data read out from line buffer 60 as per claim limitation where a first buffer memory stores the display data and a second buffer memory for storing display data being read out from the first buffer memory; an address counter for counting the readout address and the write address of said first and the second buffer memories. Perlman **discloses** display data being read out from main memory to the first buffer memory (buffer 85, Fig. 11) (...when the dispatch table is transferred to the dispatcher from the RAM 35, the data is passed through the buffer 85 and loaded into the memory 81...col. 11, lines 57-60); and a second buffer memory (buffer 102, Fig. 11) for storing the display data read out from said first buffer memory (buffer 85) (...data from the memory 81, such as the absolute origin, is coupled for each object through buffer 102 into the line buffer via the data bus 100...col. 13, lines 1-3). Perlman further **discloses** an address management element in the form of register 92, address incrementer 94, word counter 95 and adder 96 providing addresses to the RAM 35 (...as each object is selected by the decoder 90, its starting address is coupled to the register 92 and to the RAM 35 though the buffer 97 to select the first word of data for the line. If the word length for the object is fixed...the increment needed to select the first word of data for the next line is coupled through the address

incrementer 94 and adder 96 and added to the address in register 92...col. 12, lines 35-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Yiu et al. with the feature "address incrementer, word counter and adder that provides for efficient management of objects to be displayed" as taught by Perlman (col. 11, lines 36-38; 65-67; col. 12, lines 1-13) **because** it results in efficient processing of objects that are to be displayed. However, Yiu-Perlman combination **fails to disclose** processing of expansion, contraction and skip. Oh **discloses** an image data enlargement/reduction circuit comprising first and second line memories 601 and 602 for storing image data in units of one line in the main scanning direction (col. 5, lines 25-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the Yiu-Perlman combination with the feature "image expansion and contraction" as taught by Oh **because** it provides for flexible image manipulation for expansion or contraction.

b. Regarding claim 5, Yiu-Perlman combination **fails to disclose** the display control section causing the stop and motion of the readout address count to be repeated in a predetermined order. The specification of the current application refers to this process on Page 31, lines 4-18 "...for example when the data is contracted to 0.75 time,...by setting the control data for 4 pixels and the repeated point so that repetition is performed per a unit of 4 pixels, the same control data is repeatedly used to perform the contraction motion. Fig. 24 shows...where data is expanded to 1.75 times...". Oh **discloses** in Fig. 3 the image data enlargement and reduction (col. 4, lines 1-17; col. 5, lines 18-24). Oh **discloses** zoom RAM 603 access using an address generator from zoom address counter 605 by a predetermined address allocated in each area of a memory (col. 7, lines 31-44). Therefore, it would have been obvious to a person of

ordinary skill in the art at the time invention was made to modify the device as taught by Yiu-Perlman combination with the feature "predetermined address access in each area of a memory using an address generator" as taught by Oh **because** it provides for flexible arbitrary enlargement and reduction rate designated by a user.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,859,649 to Yiu et al. in view of US 5,043,714 to Perlman as applied to claim 1 above, and further in view of US 5,850,207 to Eglit.

a. Regarding claim 6, Yiu-Perlman combination is **silent about** a plurality of conversion processing circuits for converting various data formats and selection of said conversion processing circuits based on the data format. Eglit **discloses** a MVA Block 360 comprising formatter 410, color space converter 450, line buffer 430 and YUV-RGB select multiplexor 460 (col. 8, lines 52-65). Formatter 410 converts RGB 555 or 565 data into 888 format, and sends converted data over a 24-bit bus 416. Formatter 410 therefore converts received pixel data into expected pixel format. YUV-RGB select multiplexor 460 receives as input source video data in RGB 888 format on input lines 416 or 456 depending on whether source vide data is in RGB or YUV formats (col. 9, lines 64-67; col. Lines 1-5; 15-23, Fig. 4). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made of modify the device as taught by Yiu-Perlman combination with the feature "conversion processing circuits and selection of conversion processing circuits based on the data format information" as taught by Eglit **because** it provides for flexible handling of different data formats presented as inputs.

6. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,859,649 to Yiu et al. in view of US 5,043,714 to Perlman as applied to claim 1 above, and further in view of US 5,706,478 to Dye.

a. Regarding claims 7 and 8, Yiu-Perlman combination **fails to disclose** display control section is provided with a program memory and a data memory for storing the necessary programs and data; and information for program memory and data memory being transferred from said main memory. Dye **discloses** a graphics processor 100 having a private memory 116 and the graphics processor 100 transferring data between the main memory 126 and the private memory 116 (col. 7, lines 10-20). The private memory 116 is for storing up to 8 MB worth of instructions and data (col. 6, lines 30-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Yiu-Perlman with the feature "program and data memory for instructions and data" as taught by Dye **because** it provides for performance improvement as data is accessed faster from the private memory directly connected to graphics processor as opposed to data stored in main memory.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:30AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh
Examiner, Art Unit 2671

dks
February 14, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER